

WHAT IS CLAIMED IS:

- 1 1. A method of operating a switch matrix comprising:
2 configuring said switch matrix to couple a first input to a first output;
3 receiving an information stream at said first input, wherein said information
4 stream contains a plurality of portions in a sequence and a one of said
5 plurality of portions is in one position in said sequence; and
6 reconfiguring said switch matrix during a first time period, said first time
7 period corresponding to said one position in said sequence.

- 1 2. The method of claim 1, wherein said reconfiguring couples said first
2 input to a second output.

- 1 3. The method of claim 2, wherein said switch matrix is a rearrangeably
2 non-blocking switch matrix.

- 1 4. The method of claim 2, wherein said switching matrix is a CLOS
2 switching matrix.

- 1 5. The method of claim 4, wherein said method avoids generating an error
2 in other information streams transiting said switch matrix during said reconfiguring.

- 1 6. The method of claim 2, further comprising:
2 re-arranging certain ones of said plurality of portions such that said one of said
3 plurality of portions is in another position in said sequence, wherein
4 said first time period corresponds instead to said another position.

- 1 7. The method of claim 6, wherein said information stream is a SONET
2 frame.

- 1 8. The method of claim 6, wherein said first portion contains network
2 protocol overhead.

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1 9. The method of claim 6, wherein said information stream is carried by a
2 signal, further comprising:

3 loading said one of said plurality of portions with a value, said value enabling
4 said matrix to synchronize with said signal more easily.

1 10. The method of claim 2, wherein a number of said plurality of portions are
2 in various positions in said sequence, said number of said plurality of portions
3 including said one of said plurality of portions, said method further comprising:

4 re-arranging certain ones of said plurality of portions prior to said receiving
5 such that said number of said plurality of portions are in a set of
6 contiguous positions, wherein said first time period corresponds
7 instead to said set of contiguous positions.

1 11. The method of claim 10, further comprising:

2 re-arranging said certain ones of said plurality of portions such that said
3 number of said plurality of portions are in their original positions.

1 12. The method of claim 11, further comprising:

2 reading protocol information from said one of said plurality of portions during
3 said re-arranging certain ones of said plurality of portions prior to said
4 receiving;
5 processing said protocol information to derive new protocol information;
6 writing said new protocol information to said one of said plurality of portions
7 during said re-arranging said certain ones of said plurality of portions.

1 13. A method of operating a switch matrix comprising:

2 configuring said switch matrix to couple a plurality of inputs to a plurality of
3 outputs;
4 receiving a plurality of information streams at said plurality of inputs, wherein

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5 each one of said plurality of information streams comprises a plurality
6 of portions in a sequence and is received at a corresponding one
7 of said plurality of inputs,
8 for each one of said plurality of information streams,
9 a one of said plurality of portions is in a specific position of
10 said sequence, and
11 a time period during which said one of said plurality of portions
12 transits said switching matrix is at least minimally
13 concurrent with said time period for each other one of
14 said plurality of information streams, and
15 a time period of said minimal concurrency defining a switching period;
16 and
17 reconfiguring said switch matrix during said switching period.

1 14. The method of claim 13, wherein said time period of said minimal
2 concurrency is such that, for said each one of said plurality of information streams, a
3 leading edge of said one of said plurality of portions has been output from a
4 corresponding one of said plurality of outputs before a trailing edge of said one of said
5 plurality of portions is received at said corresponding one of said plurality of inputs.

1 15. The method of claim 13, wherein said configuring couples one of said
2 plurality of inputs to a one of said plurality of outputs and said reconfiguring couples
3 said one of said plurality of inputs to another of said plurality of outputs.

1 16. The method of claim 13, wherein said switch matrix is a rearrangeably
2 non-blocking switch matrix.

1 17. The method of claim 13, further comprising:
2 for certain ones of said plurality of information streams, re-arranging certain
3 ones of said plurality of portions such that said one of said plurality of
4 portions are moved to another position in said sequence of said

plurality of information streams in order to achieve said minimal concurrency.

18. The method of claim 13, wherein, for certain ones of said plurality of information streams, a number of said plurality of portions are in various positions in said sequence, said number of said plurality of portions including said one of said plurality of portions, said method further comprising,:

for said certain ones of said plurality of information streams, re-arranging certain ones of said plurality of portions prior to said receiving such that said number of said plurality of portions are in a set of contiguous positions, wherein a group time period during which said number of said plurality of portions transits said switching matrix is at least minimally concurrent with said group time period for each other one of said certain ones of said plurality of information streams.

19. The method of claim 18, further comprising:
for said certain ones of said plurality of information streams, re-arranging said certain ones of said plurality of portions such that said number of said plurality of portions are in their original positions.

20. A switching apparatus comprising:
a switching matrix, having a matrix input, a control input, and a plurality of matrix outputs, wherein said switching matrix is configured to receive an information stream at said matrix input, said information stream comprising a plurality of portions; and
control circuitry, having a control output coupled to said control input, wherein
said control circuitry is configured to initially configure said switching matrix to output said information stream at a one of said plurality of matrix outputs,
said control circuitry is configured to subsequently configure said switching matrix to output said information stream at another of

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13 said plurality of matrix outputs during a period of time during
14 which said one of said plurality of portions is transiting said
15 switching matrix.

1 21. The switching apparatus of claim 20, further comprising:
2 an input resequencing circuit, having a resequencer input and a resequencer
3 output coupled to said matrix input, wherein said input resequencing
4 circuit is configured to
5 receive said information stream at said resequencer input,
6 rearrange certain ones of said plurality of portions such that a one of
7 said plurality of portions is moved from an original position in
8 an original sequence of said plurality of portions to another
9 position in said original sequence in order to produce a
10 modified sequence of said plurality of portions, and
11 provide said information stream to said switching matrix at said input
12 resequencer output.

1 22. The switching apparatus of claim 21, further comprising:
2 a first output resequencing circuit, coupled to said one of said plurality of
3 matrix outputs, wherein said first output resequencing circuit is
4 configured to move said one of said plurality of portions from an
5 original position in said modified sequence to a position in said
6 modified sequence corresponding to said original position in said
7 original sequence; and
8 a second output resequencing circuit, coupled to said another of said plurality
9 of matrix outputs, wherein said second output resequencing circuit is
10 configured to move said one of said plurality of portions from an
11 original position in said modified sequence to a position in said
12 modified sequence corresponding to said original position in said
13 original sequence.

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6 said control circuitry is further configured to further initially configure said
7 switching matrix to couple each one of said plurality of matrix inputs
8 to a corresponding one of said plurality of matrix outputs, and
9 no errors occur in said plurality of information streams as a result of said
10 subsequent configuration of said switching matrix.

1 28. The switching apparatus of claim 20, wherein said subsequent
2 configuration of said control circuitry occurs in response to commands from control
3 software running on said control circuitry.

1 29. The switching apparatus of claim 20, wherein said subsequent
2 configuration of said control circuitry occurs in response to commands from control
3 software running on a route processor coupled to said control circuitry.

1 30. A switching apparatus comprising:
2 an input resequencing circuit, having a resequencer input and a resequencer
3 output, wherein said first resequencing circuit is configured to
4 receive an information stream comprising a plurality of portions at said
5 resequencer input, each one of said plurality of portions
6 comprising a plurality of sub-portions, and
7 move a one of said plurality of sub-portions of said each one of said
8 plurality of portions from an original position in a sequence of
9 said each one of said plurality of portions to another position in
10 said sequence, and
11 output said information stream at said resequencer output;
12 a switching matrix, having a matrix input coupled to receive said information
13 stream from said resequencer output, a control input, and a plurality of
14 matrix outputs; and
15 control circuitry, having a control output coupled to said control input,
16 wherein said control circuitry is configured to cause said switching
17 matrix to switch said information stream from said one of said plurality

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18 of matrix outputs to another of said plurality of matrix outputs during a
19 period of time corresponding to said another position.

1 31. The switching apparatus of claim 30, further comprising:
2 a first output resequencing circuit, coupled to said one of said plurality of
3 matrix outputs and configured to move said one of said plurality of
4 sub-portions of said each one of said plurality of portions from said
5 another position in said sequence to said original position in said
6 sequence; and
7 a second output resequencing circuit, coupled to said another of said plurality
8 of matrix outputs and configured to move said one of said plurality of
9 sub-portions of said each one of said plurality of portions from said
10 another position in said sequence to said original position in said
11 sequence.

1 32. The switching apparatus of claim 30, wherein said switching matrix is
2 a re-arrangeably non-blocking switching matrix.

1 33. The switching apparatus of claim 30, wherein said one of said portions
2 is expendable.

1 34. The switching apparatus of claim 30, wherein said one of said plurality
2 of portions contains protocol overhead information.

1 35. The switching apparatus of claim 30, wherein
2 said matrix input is one of a plurality of matrix inputs,
3 said information stream is one of a plurality of information streams,
4 each one of said plurality of information streams is received at a corresponding
5 one of said plurality of matrix inputs,
6 said control circuitry is further configured to further initially configure said
7 switching matrix to couple each one of said plurality of matrix inputs
8 to a corresponding one of said plurality of matrix outputs, and

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- 9 no errors occur in said plurality of information streams as a result of said
10 subsequent configuration of said switching matrix.

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